We claim:

1. A method of fabricating a CMOS have self-aligned shallow trench isolation, comprising:

preparing a silicon substrate, including forming well structures therein to provide an active area;

forming a gate stack, including forming a gate insulation layer;

depositing a layer of first polysilicon to a thickness $T_{P1} \pm \Delta T_{P1}$, where T_{P1} is the desired thickness of the first polysilicon layer and ΔT_{P1} is the variation of the thickness of the first polysilicon layer;

trenching the substrate by shallow trench isolation to form a trench having a depth $X_{STI} \pm \Delta X_{STI}$, where X_{STI} is the desired depth of the trench and ΔX_{STI} is the variation of the depth of the trench;

filling the trench with oxide to form a field oxide to a depth of $T_{OX} \pm \Delta T_{OX}$, where T_{OX} is the desired thickness of the oxide ΔT_{OX} is the variation of the thickness of the oxide;

depositing a second layer of polysilicon to a thickness $T_{P2} \pm \Delta T_{P2}$, where T_{P2} is the desired thickness of the second polysilicon layer and ΔT_{P2} is the variation of the thickness of the second polysilicon layer, and wherein the top surface of the second polysilicon layer is above the top surface of the first polysilicon layer, and wherein $T_{P2} - \Delta T_{P2} + T_{OX} - \Delta T_{OX} > X_{STI} + \Delta X_{STI} + T_{P1} + \Delta T_{P1}$;

depositing a sacrificial oxide layer having a thickness of at least 1.5X that of the first and second polysilicon layers;

CMP the sacrificial oxide layer to the level of the upper surface of the

second polysilicon layer;

depositing a third layer of polysilicon;

patterning and etching the gate stack;

implanting ions to form a source region, a drain region and the polysilicon gate; and

completing the CMOS structure.

2. The method of claim 1 which includes, after said CMP of the sacrificial oxide, selectively etching any remaining oxide on the top surface of the first polysilicon layer.

3. The method of claim 1 wherein said patterning and etching includes a two-step plasma etching process, including removing the overlying sacrificial oxide and that portion of the second polysilicon layer in the active areas with a non-selective slurry, and selectively polishing the structure to removes the remaining sacrificial oxide, stopping at the level of the second polysilicon layer in the field are without polishing the field oxide.

4. The method of claim 1 wherein said filling the trench with oxide includes filling the trench with an oxide taken from the group of oxides consisting of silicon oxide, silicon oxynitride, and a high-k dielectric taken from the group of high-k dielectrics consisting of hafnium oxide, zirconium oxide, lanthanum oxide, aluminum oxide, their silicates, and other suitable insulating material.

5. A method of fabricating a CMOS have self-aligned shallow trench isolation, comprising:

preparing a silicon substrate, including forming well structures therein to provide an active area;

forming a gate stack, including forming a gate insulation layer;

depositing a first polysilicon layer to a thickness $T_{P1} \pm \Delta T_{P1}$, where T_{P1} is the desired thickness of the first polysilicon layer and ΔT_{P1} is the variation of the thickness of the first polysilicon layer;

trenching the substrate by shallow trench isolation to form a trench having a depth $X_{STI} \pm \Delta X_{STI}$, where X_{STI} is the desired depth of the trench and ΔX_{STI} is the variation of the depth of the trench;

filling the trench with oxide to form a field oxide to a depth of $T_{OX} \pm \Delta T_{OX}$, where T_{OX} is the desired thickness of the oxide ΔT_{OX} is the variation of the thickness of the oxide;

depositing a second layer of polysilicon to a thickness $T_{P2} \pm \Delta T_{P2}$, where T_{P2} is the desired thickness of the second polysilicon layer and ΔT_{P2} is the variation of the thickness of the second polysilicon layer, and wherein the top surface of the second polysilicon layer is above the top surface of the first polysilicon layer, and wherein $T_{P2} - \Delta T_{P2} + T_{OX} - \Delta T_{OX} > X_{STI} + \Delta X_{STI} + T_{P1} + \Delta T_{P1}$;

depositing a sacrificial oxide layer having a thickness of at least 1.5X that of the first and second polysilicon layers;

CMP the sacrificial oxide layer to the level of the upper surface of the second polysilicon layer;

removing the first and second polysilicon layers;

forming a dielectric layer;

forming a damascene gate structure

depositing a third layer of polysilicon;

patterning and etching the gate stack;

implanting ions to form a source region, a drain region and the polysilicon gate; and

completing the CMOS structure.

6. The method of claim 5 wherein said patterning and etching includes a two-step plasma etching process, including removing the overlying sacrificial oxide and that portion of the second polysilicon layer in the active areas with a non-selective slurry, and selectively polishing the structure to removes the remaining sacrificial oxide, stopping at the level of the second polysilicon layer in the field are without polishing the field oxide.

7. The method of claim 6 wherein said filling the trench with oxide includes filling the trench with an oxide taken from the group of oxides consisting of silicon oxide, silicon oxynitride, and a high-k dielectric taken from the group of high-k dielectrics consisting of hafnium oxide, zirconium oxide, lanthanum oxide, aluminum oxide, their silicates, and other suitable insulating material.

8. A method of fabricating a CMOS have self-aligned shallow trench isolation, comprising:

preparing a silicon substrate, including forming well structures therein to provide an active area;

forming a gate stack, including forming a gate insulation layer;

depositing a layer of first polysilicon to a thickness $T_{P1} \pm \Delta T_{P1}$, where T_{P1} is the desired thickness of the first polysilicon layer and ΔT_{P1} is the variation of the thickness of the first polysilicon layer;

trenching the substrate by shallow trench isolation to form a trench having a depth $X_{STI} \pm \Delta X_{STI}$, where X_{STI} is the desired depth of the trench and ΔX_{STI} is the variation of the depth of the trench;

filling the trench with oxide to form a field oxide to a depth of $T_{OX} \pm \Delta T_{OX}$, where T_{OX} is the desired thickness of the oxide ΔT_{OX} is the variation of the thickness of the oxide;

depositing a second layer of polysilicon to a thickness $T_{P2} \pm \Delta T_{P2}$, where T_{P2} is the desired thickness of the second polysilicon layer and ΔT_{P2} is the variation of the thickness of the second polysilicon layer, and wherein the top surface of the second polysilicon layer is above the top surface of the first polysilicon layer, and wherein $T_{P2} - \Delta T_{P2} + T_{OX} - \Delta T_{OX} > X_{STI} + \Delta X_{STI} + T_{P1} + \Delta T_{P1}$;

depositing a sacrificial oxide layer having a thickness of at least 1.5X that of the first and second polysilicon layers;

CMP the sacrificial oxide layer to the level of the upper surface of the second polysilicon layer;

selectively etching the oxide;

depositing a third layer of polysilicon to form an alignment key at the edge of the trench;

patterning and etching the gate stack;

implanting ions to form a source region, a drain region and the polysilicon gate; and

completing the CMOS structure.

9. The method of claim 8 which includes, after said CMP of the sacrificial oxide, selectively etching any remaining oxide on the top surface of the first polysilicon layer.

10. The method of claim 8 wherein said patterning and etching includes a two-step plasma etching process, including removing the overlying sacrificial oxide and that portion of the second polysilicon layer in the active areas with a non-selective slurry, and selectively polishing the structure to removes the remaining sacrificial oxide, stopping at the level of the second polysilicon layer in the field are without polishing the field oxide.

11. The method of claim 8 wherein said filling the trench with oxide includes filling the trench with an oxide taken from the group of oxides consisting of silicon oxide, silicon oxynitride, and a high-k dielectric taken from the group of high-k dielectrics consisting of hafnium oxide, zirconium oxide, lanthanum oxide, aluminum oxide, their silicates, and other suitable insulating material.

12. A method of fabricating a CMOS have self-aligned shallow trench isolation, comprising:

preparing a silicon substrate, including forming well structures therein to provide an active area;

forming a gate stack, including forming a gate insulation layer;

depositing a layer of first polysilicon to a thickness $T_{P1} \pm \Delta T_{P1}$, where T_{P1} is the desired thickness of the first polysilicon layer and ΔT_{P1} is the variation of the thickness of the first polysilicon layer;

trenching the substrate by shallow trench isolation to form a trench having a depth $X_{STI} \pm \Delta X_{STI}$, where X_{STI} is the desired depth of the trench and ΔX_{STI} is the variation of the depth of the trench;

filling the trench with oxide to form a field oxide to a depth of $T_{OX} \pm \Delta T_{OX}$, where T_{OX} is the desired thickness of the oxide ΔT_{OX} is the variation of the thickness of the oxide;

depositing a sacrificial oxide layer having a thickness of at least 1.5X that of the first polysilicon layer;

CMP the sacrificial oxide layer to the level of the upper surface of the second polysilicon layer;

depositing a capping polysilicon layer to form an alignment key at the edge of the trench;

patterning and etching the gate stack;

implanting ions to form a source region, a drain region and the polysilicon gate; and

completing the CMOS structure.

13. The method of claim 12 which includes, after said CMP of the sacrificial oxide, selectively etching any remaining oxide on the top surface of the first polysilicon layer.

14. The method of claim 12 wherein said patterning and etching includes a two-step plasma etching process, including removing the overlying sacrificial oxide and that portion of the second polysilicon layer in the active areas with a non-selective slurry, and selectively polishing the structure to removes the remaining sacrificial oxide, stopping at the level of the second polysilicon layer in the field are without polishing the field oxide.

15. The method of claim 12 wherein said filling the trench with oxide includes filling the trench with an oxide taken from the group of oxides consisting of silicon oxide, silicon oxynitride, and a high-k dielectric taken from the group of high-k dielectrics consisting of hafnium oxide, zirconium oxide, lanthanum oxide, aluminum oxide, their silicates, and other suitable insulating material.